[What is Claimed is]

1. A process for a semiconductor integrated circuit device where a plurality of memory cells which have field effect transistors formed in a semiconductor substrate and capacitor elements connected to the source and drain regions of said field effect transistors are provided, comprising the steps of:

(a) forming trenches of which the radius of curvature of the bottom corners is larger than 10nm in said semiconductor substrate;

(b) forming a first gate insulating film through a deposition method inside of said trenches; and

(c) forming gate electrodes within said trenches and placing said gate electrodes on said first gate insulating film

2. A process for a semiconductor integrated circuit device according to Claim 1 characterized by having the step of forming a second gate insulating film by oxidizing the inner walls of said trenches.

3. A process for a semiconductor integrated circuit device according to Claim 1, wherein the step of forming said trenches contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the

trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy.

4. A process for a semiconductor integrated circuit device, at the time of forming field effect transistors in a semiconductor substrate, comprising the steps of:

(a) forming trenches in said semiconductor substrate;

(b) forming a gate insulating film inside of said trenches;

(c) forming gate electrodes which are completely, or partially, buried within said trenches under the condition where said gate insulating film is interposed between said gate electrodes and said semiconductor substrate within said trenches; and

(d) forming semiconductor regions for the sources and drains in said semiconductor substrate, wherein

said Step (a) contains the step of rounding the bottom corners within said trenches so that the sub-threshold coefficient of said field effect transistors does not exceed a predetermined value, and

said Step (b) contains the step of forming said

gate insulating film through a deposition method.

5. A process for a semiconductor integrated circuit device according to Claim 4, wherein said Step (a) contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy.

6. A process for a semiconductor integrated circuit device according to Claim 4, wherein said Step (b) contains the step of forming part of said gate insulating film by oxidizing the inner walls of said trenches.

7. A process for a semiconductor integrated circuit device according to Claim 4, wherein the radius of curvature of the bottom corners within said trenches is 10nm or more.

8. A process for a semiconductor integrated circuit device which has element isolation parts and wires formed so as to cross over said element isolation parts within a semiconductor substrate are provided, comprising the steps of:

(a) forming a first trench in said semiconductor

substrate;

(b) forming element isolation parts by forming an insulating film in said first trench;

(c) forming a mask which has apertures crossing over said element isolation parts;

(d) forming a second trench in the element isolation parts which have been exposed through said apertures;

(e) forming a third trench in the semiconductor substrate which has been exposed through said apertures and the second trench; and

(f) forming said wires in said second and third trenches.

9. A process for a semiconductor integrated circuit device according to Claim 8, wherein the inclination angle of the side walls of said first and third trenches, with respect to the main surface of said semiconductor substrate, is smaller than 90 degrees.

10. A process for a semiconductor integrated circuit device which has element isolation parts formed within a semiconductor substrate, a first wire formed so as to cross over said element isolation parts and field effect transistors having part of said first wire as gate electrodes and having source and

drain regions on both sides of said gate electrodes are provided, comprising the steps of:

(a) forming a first trench by etching said semiconductor substrate;

(b) forming element isolation parts by forming an insulator film inside of said first trench;

(c) forming a mask which has first apertures formed so as to cross over said element isolation parts;

(d) forming a second trench by etching the element isolation parts which have been exposed through said first apertures;

(e) forming a third trench by etching the semiconductor substrate which has been exposed through said first apertures and said second trench; and

(f) forming a gate insulating film on the inside walls of said third trench and forming the first wire inside of said second and third trenches.

11. A process for a semiconductor integrated circuit device according to Claim 10, wherein the inclination angle of the side walls of said first and third trenches, with respect to the main surface of said semiconductor substrate, is smaller than 90 degrees.

12. A process for a semiconductor integrated

circuit device according to Claim 10, wherein forward tapers are formed on the side surfaces of said first and third trenches.

13. A process for a semiconductor integrated circuit device according to Claim 10, wherein said first trench is 100nm, or more, deeper than said second trench.

14. A process for a semiconductor integrated circuit device according to Claim 10, wherein said step of forming the third trench further contains the step of oxidizing the inner walls of the trench formed through etching of said semiconductor substrate and the step of removing the oxide film formed according to said oxidation.

15. A process for a semiconductor integrated circuit device according to Claim 10, wherein said third trench is deeper than said second trench.

16. A process for a semiconductor integrated circuit device according to Claim 10, wherein said first trench is deeper than said third trench.

17. A process for a semiconductor integrated circuit device is provided, comprising the steps of:

(a) forming a first trench in a semiconductor substrate;

(b) forming isolation parts by forming an

insulating film for isolation in said first trench;

(c) forming a mask having aperture parts which expose both of said isolation parts and said semiconductor substrate on said semiconductor substrate;

(d) forming a second trench in the isolation parts which have been exposed from said aperture parts and, after that, forming a third trench in the semiconductor substrate which has been exposed from said aperture parts and said second trench;

(e) forming an insulating film on the surface of the semiconductor substrate within said second and third trenches; and

(f) forming wires within said second and third trenches.

18. A process for a semiconductor integrated circuit device according to Claim 17, wherein at the time of forming said second trench, at the stage after said Step (f), said insulating film for isolation remains at the bottom of said second trench so that no parasitic elements are formed below the wires formed inside of said second trench.

19. A process for a semiconductor integrated circuit device according to Claim 17, wherein at the stage after said Step (f), the thickness of said

insulating film for isolation which remains between the wires inside of said second trench and the semiconductor substrate is 100nm or more.

20. A process for a semiconductor integrated circuit device according to Claim 17, wherein at the time of forming said third trench, the depth of said third trench is deeper than said second trench.

21. A process for a semiconductor integrated circuit device according to Claim 17, wherein the dimensions of the aperture sides of said first and third trenches are greater than the dimensions of the bottom sides.

22. A process for a semiconductor integrated circuit device according to Claim 21, wherein forward tapers are formed on the side surfaces of said first and third trenches.

23. A process for a semiconductor integrated circuit device according to Claim 17 characterized by having the oxidation step for oxidizing the inside of said second and third trenches after said Step (d) and before said Step (e) and the step of removing the oxide film which has been formed through said oxidation step.

24. A process for a semiconductor integrated circuit device according to Claim 23, wherein said

Step (e) contains the step of forming said insulating film through a deposition method.

25. A process for a semiconductor integrated circuit device according to Claim 23, wherein the process for forming an insulating film in said Step (e) contains the step of forming a first gate insulating film by oxidizing the surface of said semiconductor substrate and the step of forming a second gate insulating film, through a deposition method, so as to cover the surface of said first gate insulating film.

26. A process for a semiconductor integrated circuit device according to Claim 17, wherein said step of forming wires comprises the steps of: filling in said second and third trenches with a first film for forming said wires; removing said first film so that a part thereof remains inside of said second and third trenches; forming a second film which fills in the recesses of the surface of the first film which has remained inside of said second and third trenches; and removing said first film, after the formation of said second film, so that a part thereof remains inside of said second and third trenches.

27. A process for a semiconductor integrated circuit device according to Claim 26 characterized by

having the step of forming a first insulating film on the wires inside of said second and third trenches by removing the first insulating film so that a part thereof remains inside of said second and third trenches after depositing the first insulating film on said semiconductor substrate subsequent to the formation of said wires.

28. A process for a semiconductor integrated circuit device according to Claim 27 characterized by having the step of depositing a second insulating film on said semiconductor substrate after forming said first insulating film inside of the second and third trenches, and forming holes which expose part of said semiconductor substrate in said second insulating film, wherein:
in said step of forming holes, said holes are formed by carrying out an etching process under conditions where the etching rate of said second insulating film is faster than that of said first insulating film.

29. A process for a semiconductor integrated circuit device according to Claim 28, wherein after filling in said holes with a conductive film, semiconductor regions are formed in a semiconductor substrate through impurity diffusion into the semiconductor substrate from the conductive film.

30. A process for a semiconductor integrated circuit device according to Claim 17, wherein said wires have a polycrystal silicon film, a silicide film or a metal film, or a laminated film of these.

31. A process for a semiconductor integrated circuit device according to Claim 17, wherein the insulating film of said Step (e) forms a gate insulating film for field effect transistors while the wires of said Step (f) form gate electrodes for said field effect transistors.

32. A process for a semiconductor integrated circuit device according to Claim 17 characterized by having the step of forming pairs of semiconductor regions for sources and drains of said field effect transistors in an active region surrounded by the isolation parts of said semiconductor substrate after said Step (f) and the step of forming capacitor elements for information storage which are connected to either one of the semiconductor regions of said pairs.

33. A process for a semiconductor integrated circuit device is provided, comprising the steps of:

(a) forming element isolation parts in a semiconductor substrate;

(b) forming a mask having apertures over said

semiconductor substrate;

(c) forming a first trench in the semiconductor substrate which has been exposed from said apertures;

(d) forming a first film in said first trench;

(e) removing part of said first film so that part of said first film remains in said first trench; and

(f) forming a second film so as to fill in recesses on the surface of said first film.

34. A process for a semiconductor integrated circuit device which has a plurality of memory cells having field effect transistors with buried gate electrodes formed in a semiconductor substrate and capacitor elements electrically connected to at least one of the source or drain regions of said field effect transistors are provided, comprising the steps of:

(a) forming first semiconductor regions in said semiconductor substrate;

(b) forming a first trench in said semiconductor substrate;

(c) forming a gate insulating film, gate electrodes and a first insulating film inside said first trench;

(d) forming a second insulating film on the

semiconductor substrate and, further, on said first insulating film;

(e) forming apertures, in said second insulating film, which overlap said first semiconductor regions in a plane manner through a method where the etching rate of said second insulating film is faster than the etching rate of the first insulating film;

(f) forming a conductive film inside of said apertures; and

(g) forming second semiconductor regions in said semiconductor substrate through an impurity diffusion from said conductive film and of forming said source and drain regions of said first and second semiconductor regions.

35. A process for a semiconductor integrated circuit device according to Claim 34, wherein said first insulating film is formed of a silicon nitride film and said second insulating film is formed of a silicon oxide film.

36. A semiconductor integrated circuit device having field effect transistors formed in a semiconductor substrate, wherein said field effect transistors have trenches formed in said semiconductor substrate, a gate insulating film which is formed inside of said trenches, gate electrodes which are

formed on said gate insulating film and source and drain regions which are formed in the semiconductor substrate on both sides of said gate electrodes and wherein said gate insulating film is formed through a deposition method and said trenches have the radius of curvature of the bottom corners of 10nm or more.

37. A semiconductor integrated circuit device according to Claim 36 characterized by having a plurality of memory cells which have said field effect transistors and capacitor elements connected to said source and drain regions.

38. A semiconductor integrated circuit device having field effect transistors formed in a semiconductor substrate, wherein said field effect transistors have trenches formed in said semiconductor substrate, a gate insulating film formed inside of said trenches, gate electrodes formed on said gate insulating film and source and drain regions formed in the semiconductor substrate on both sides of said gate electrodes and wherein said gate insulating film is formed through a deposition method and the radius of curvature of the bottom corners of said trenches in the channel forming regions between said source and drain regions is larger than 10nm.

39. A semiconductor integrated circuit device

characterized by having field effect transistors which include trenches formed in a semiconductor substrate, a gate insulating film formed inside of said trenches and gate electrodes completely, or partially, buried inside of said trenches under the conditions where said gate insulating film is interposed between the gate electrodes and the semiconductor substrate within said trenches, wherein said gate insulating film has an insulating film formed through a deposition method and the bottom corners within said trenches are rounded.

40. A semiconductor integrated circuit device having a plurality of memory cells which have field effect transistors of a buried gate electrode type and capacitor elements electrically connected to, at least, one of the source or drain regions of said field effect transistors in a semiconductor substrate, wherein said semiconductor substrate has first semiconductor regions of which the conductivity type is the opposite of said source and drain regions and which are formed up to positions deeper than said buried gate electrodes, and wherein the source and drain regions connected to said capacitor elements have second semiconductor regions formed up to positions shallower than the first semiconductor

regions and third semiconductor regions formed up to positions shallower than said second semiconductor regions wherein the impurity concentration of said third semiconductor regions is higher than the impurity concentration of said second semiconductor regions.

41. A semiconductor integrated circuit device characterized by having a gate insulating film, gate electrodes on said gate insulating film and a first insulating film on said gate electrodes within a first trench formed in a semiconductor substrate and by having first semiconductor regions of a first conductive type formed up to positions deeper than said first trench, second semiconductor regions of a conductive type opposite to said first conductive type formed above said first semiconductor regions and third semiconductor regions of the same conductive type as that of said second semiconductor regions formed above said second semiconductor regions, wherein the impurity concentration of said third semiconductor regions is higher than the impurity concentration of said second semiconductor regions.

42. A semiconductor integrated circuit device according to Claim 41, wherein the borders between said third semiconductor regions and second

semiconductor regions are formed in positions shallower than the top surfaces of said gate electrodes.

43. A semiconductor integrated circuit device according to Claim 42, wherein the borders between said third semiconductor regions and second semiconductor regions are formed in positions apart from the top parts of said gate electrodes.

44. A semiconductor integrated circuit device according to Claim 43, wherein the distance between the borders, between said third semiconductor regions and second semiconductor regions, and said gate electrodes is 40nm or more.

45. A semiconductor integrated circuit device according to Claim 41, wherein the borders between said first semiconductor regions and second semiconductor regions are formed in positions deeper than the top surfaces of said gate electrodes.

46. A semiconductor integrated circuit device having a plurality of memory cells which have field effect transistors of a buried gate electrode type and capacitor elements electrically connected to, at least, one of the source or drain regions of said field effect transistors, wherein a buried gate cap insulating film is formed on the buried gate

electrodes of said field effect transistors and the thickness of said buried gate cap insulating film is 40nm or more.

47. A semiconductor integrated circuit device having a plurality of memory cells which have field effect transistors of a buried gate electrode type and capacitor elements electrically connected to, at least, one of the source or drain regions of said field effect transistors, wherein the source or drain regions to which said capacitor elements are connected are formed deeper than the other source or drain regions.

48. A semiconductor integrated circuit device having a plurality of memory cells which have field effect transistors of a buried gate type and capacitor elements electrically connected to, at least, one of the source or drain regions of said field effect transistors, wherein the semiconductor integrated circuit device has a peripheral circuit region which has field effect transistors of a buried gate electrode type wherein the source and drain regions of field effect transistors in said peripheral circuit region are formed deeper than the source and drain regions of the field effect transistors of said memory cells.

49. A semiconductor integrated circuit device having field effect transistors which have buried gate electrodes formed in a semiconductor substrate, wherein said gate electrodes are formed of a metal or a metal silicide film and the gate insulating film of said field effect transistors has an insulating film formed through a deposition method.

50. A semiconductor integrated circuit device characterized by having a first trench formed in a semiconductor substrate, isolation parts formed by filling in the inside of said first trench with an insulating film, a trench for forming wires which is arranged so as to overlap said semiconductor substrate and isolation parts in a plane manner and which is formed by excavating said semiconductor substrate and isolation parts, a gate insulating film formed on the surface of the semiconductor substrate within said trench for forming wires, said wires formed within said trench under the condition where a gate insulating film is interposed between the wires and said semiconductor substrate and a cap insulating film formed on said wires within said trench for forming wires, wherein said gate insulating film has an insulating film formed through a deposition method.